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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,318	12/18/2001	Joon Ki Hong	10729-P67426US0	8219

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EXAMINER
HA, NATHAN W

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,318	HONG, JOON KI	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-3, 7, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Horton et al. (US 6,326,696, previously cited, hereinafter, "Horton".)

In regard to claims 1 and 10, in fig. 1, Horton discloses a stack chip module 10 including:

a substrate 12 having a predetermined-size groove or cavity 14 on one side and a circuit pattern 19 with one end being adjacent to the groove;

a first semiconductor chip 16 adhered in the groove of the substrate by adhesive 22 and having a plurality of center pads, also, 26 and a plurality of edge pads 26, electrically connected to each other, on an upper part thereof, see also corresponding text on col. 3, lines 1-50;

a plurality of metal wires 20 for electrically connecting the circuit pattern of the substrate and the edge pads of the first chip, respectively;

a second semiconductor chip18 having a plurality of center pads, also numbered as 26, corresponding to the plurality of the center pads on the upper part of the first chip and the formative side being opposite to that of the first chip;

a plurality of the bumps, also 26 interposed between the center pads of the first and second chips for joining and electrically connecting the center pads; and

a molding 28 at the sides of the second semiconductor chip including the gold wires, the edge pads of the first chip, and the circuit patterns of the substrate, see also, col. 3, lines 21-22.

In regard to claim 2, Horton further discloses that the second chip has a size that fits inside of the edge pads of the first chip and the height of the solder bumps.

In regard to claim 3, the bumps or columns 26 are made of solder bumps or gold bumps, see also, col. 3, lines 25-27.

In regard to claim 7, a heat sink 32 is attached to the bottom of the groove; see fig. 2.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horton as applied to claims 1-3 above.

Horton as discussed above discloses all of the claimed limitations. However, despite the drawings therein, Horton does not expressly mention an accurate height of the bumps in the corresponding text.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the size of the second chip and adjust the height of the bumps because applicant has not disclosed that this size provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either size because it performs the same function of a stack chip and electrically connecting between the chips.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Horton's in order to obtain the invention as specified in claim 4.

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horton as applied to claims 1-4 above, and further in view of Ference et al. (US 6,265,771, previously cited, herein after, "Ference".)

In regard to claim 5, Horton discloses all of the claimed limitations as mention above except a heat sink on the second stack chip. Ference, in fig. 4, discloses a stack ship device having first chip 12, a smaller second chip 16 on top of the first chip and further a heat sink 26 is attached to the back of the second chip so the heat can dissipated through an exposed surface through this heart sink, therefore, transferring heat away from the other chip; see also, col. 3, lines 10-25.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Horton as taught by Ference in order to obtain the advantage mentioned above.

6. Claims 6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horton as applied to claim 1 above, and further in view of Chan et al. (US 6,326,696, previously cited, hereinafter "Chan".)

In regard to claim 6, Horton discloses all of the claimed limitations as mention above and further discloses that the substrate is a printed circuit board that carries semiconductor chips. Horton, however, does not expressly mention that the substrate can be put into a socket and arranged on both sides in a jig-jag form.

Chan, in figs. 2 and 5, discloses an analogous semiconductor package which is similar to the instant invention including chips, for example, 50 in the grooves therein. Chan further teaches the chips are placed in the grooves of the circuit board 70 on the both sides of the board in a jig-jag form. At the final assembly this board will be plugged in a motherboard socket. The double-sided substrate is normally used to achieve high-speed performance and to meet the space constraint requirements of modern semiconductors, see Chan's col. 3, lines 4-14.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Horton as taught by Chan in order to obtain the advantages as mentioned above.

Response to Arguments

7. Applicant's arguments filed 6/24/03 have been fully considered but they are not persuasive. For instance, Applicants submit that Horton does not teach the center pads on the chips 16 and 18. It is noted that pad connections are necessary in the solder bump connections since pads provide electrical contact to the circuits or devices therein, and provide a base for the electrical bumps. Therefore, pads are inherently disclosed by Horton in fig. 1, for example. Horton however, discloses the contact pads 52 and 54 in figs. 5a-5b for electrical connection to the substrate. The pads 54 are arranged in the central array for connections through bump 26 as shown in fig. 1; see col. 4, lines 40-47.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (703) 305-3507. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and 308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha
July 14, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800